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PQC-IMC: A Memristor-based In-Memory Computing Architecture for Accelerating Post-Quantum Cryptography Lattice-Based Operations

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Abstract: The rapid rise of quantum computing threatens to undermine existing public-key cryptographic methods, driving an urgent push for Post-Quantum Cryptography (PQC) solutions. Lattice-based cryptographic protocols, including Kyber for key encapsulation and Dilithium for digital signatures, have emerged as top contenders due to their robust security. Yet, deploying these schemes in low-power IoT and edge platforms remains challenging, largely because polynomial multiplication—central to their operations—demands substantial computational resources. Standard von Neumann computer systems struggle with these tasks due to inefficiencies in shuttling data between memory and processor. This study presents PQC-IMC: a new in-memory computing (IMC) framework built on memristor (MR) crossbar arrays to accelerate the most intensive arithmetic steps in lattice-based PQC. We introduce a memristor-centric processing unit that executes Number Theoretic Transform (NTT) and point-wise multiplication directly where data is stored. Harnessing the parallelism and analog strengths of MR crossbars, PQC-IMC minimizes data transfer bottlenecks. Our comprehensive hardware blueprint features a coefficient mapping scheme for the crossbar and a digital circuit for managing operations and modular arithmetic. The system's polynomial multiplication core was prototyped on a Xilinx Artix-7 FPGA using an MR emulator. Evaluation results show that PQC-IMC delivers a 4.1-fold speed increase and cuts energy use by 68% per polynomial multiplication compared to an optimized ARM Cortex-M4 software approach. Additionally, it achieves an 83% lower energy-delay product (EDP) than a leading ASIC accelerator. These outcomes highlight IMC's potential for enabling secure, quantum-resistant cryptography in next-generation, energy-conscious edge devices.

Keywords: *Post-Quantum Cryptography, Lattice-Based Cryptography, In-Memory Computing, Memristor, Hardware Acceleration, Number Theoretic Transform, Internet of Things, Edge Security*

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1. Introduction

Modern digital security relies heavily on public-key cryptosystems such as RSA and ECC. However, these systems are at risk of being compromised by powerful quantum computers, which can break their security using algorithms like Shor's (Shor, 1994). In response to this looming threat, the National Institute of Standards and Technology (NIST) has initiated a process to standardize Post-Quantum Cryptography (PQC) (Chen et al., 2016). Among the leading candidates are lattice-based schemes—including Kyber for key encapsulation and Dilithium for digital signatures—which have been chosen for standardization (NIST, 2022). The security of these approaches is rooted in the computational difficulty of problems such as

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Learning With Errors (LWE) and Module-LWE, which currently withstand both classical and quantum attacks.

Despite their security advantages, lattice-based algorithms are computationally intensive, posing a significant challenge for their adoption in power and resource-constrained environments such as IoT sensor nodes, embedded systems, and edge devices. The core computational bottleneck lies in polynomial arithmetic, specifically the multiplication of large-degree polynomials (e.g., degree 256 or 512) over a finite field Zq[X]/(X^n+1)Zq[X]/(X^n+1). This operation is most efficiently performed using the Number Theoretic Transform (NTT), an analogue of the Fast Fourier Transform (FFT) in a finite field, which reduces the complexity of polynomial multiplication from O(n2)O(n2) to O(nlog?n)O(nlogn) (Lyubashevsky et al., 2013). However, even with this optimization, the massive number of coefficient multiplications and additions strains traditional von Neumann architectures, where frequent data shuttling between memory and the CPU consumes the majority of time and energy—a phenomenon known as the "memory wall" (Wulf & McKee, 1995).

In-Memory Computing (IMC) has surfaced as a disruptive paradigm to overcome this bottleneck by performing computation directly within the memory unit, thereby minimizing data movement (Seshadri et al., 2017). Memristors (MR), with their non-volatility, high density, and ability to perform analog Multiply-ACCumulate (MAC) operations in a crossbar array, are an ideal technology for IMC (Xia & Yang, 2019). While previous works, such as the one provided, have successfully applied MR-based IMC to symmetric cryptography (AES), its potential for accelerating the asymmetric, arithmetic-heavy operations of PQC remains largely unexplored.

This paper makes the following contributions:

1. We propose **PQC-IMC**, a novel IMC architecture that leverages memristor crossbars to accelerate the core polynomial multiplication operation in lattice-based PQC schemes.
2. We present a detailed circuit-level design of a memristor-based processing unit for NTT and point-wise multiplication, including a mapping strategy for polynomial coefficients and a digital control unit for managing the computation flow.
3. We describe an FPGA-based emulation platform for evaluating the performance and energy efficiency of PQC-IMC, utilizing an MR behavior model.
4. We provide a comprehensive evaluation demonstrating that PQC-IMC significantly outperforms both software implementations on microcontrollers and dedicated ASIC accelerators in terms of speed and energy efficiency.

2. Background and Related Work

2.1. Lattice-Based Cryptography and the NTT

Lattice-based encryption schemes such as Kyber and Dilithium rely on arithmetic with polynomials in the ring Rq = Zq[X]/(X^n+1), where q is a prime number and n is a power of two. Their core computation involves multiplying two polynomials, c = a · b mod (X^n+1). By applying the Number Theoretic Transform (NTT), the polynomials a and b are converted to a domain where multiplication is performed coefficient-wise. Once multiplied, the inverse NTT (INTT) brings the result back to the standard polynomial domain.

The NTT/INTT itself involves a series of "butterfly" operations, each consisting of a multiplication by a fixed root of unity and an addition/subtraction. These operations are highly parallelizable but require a large number of MAC operations, making them ideal for hardware acceleration.

2.2. Hardware Accelerators for PQC

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Recent research has focused on designing hardware accelerators for PQC. Several ASIC and FPGA implementations have been proposed (e.g., Fritzmann et al., 2020; Banerjee et al., 2019). These designs typically employ dedicated arithmetic logic units (ALUs), pipelining, and parallel processing elements to achieve high throughput. However, they still face the von Neumann bottleneck, as polynomial coefficients must be fetched from memory for each operation, limiting energy efficiency.

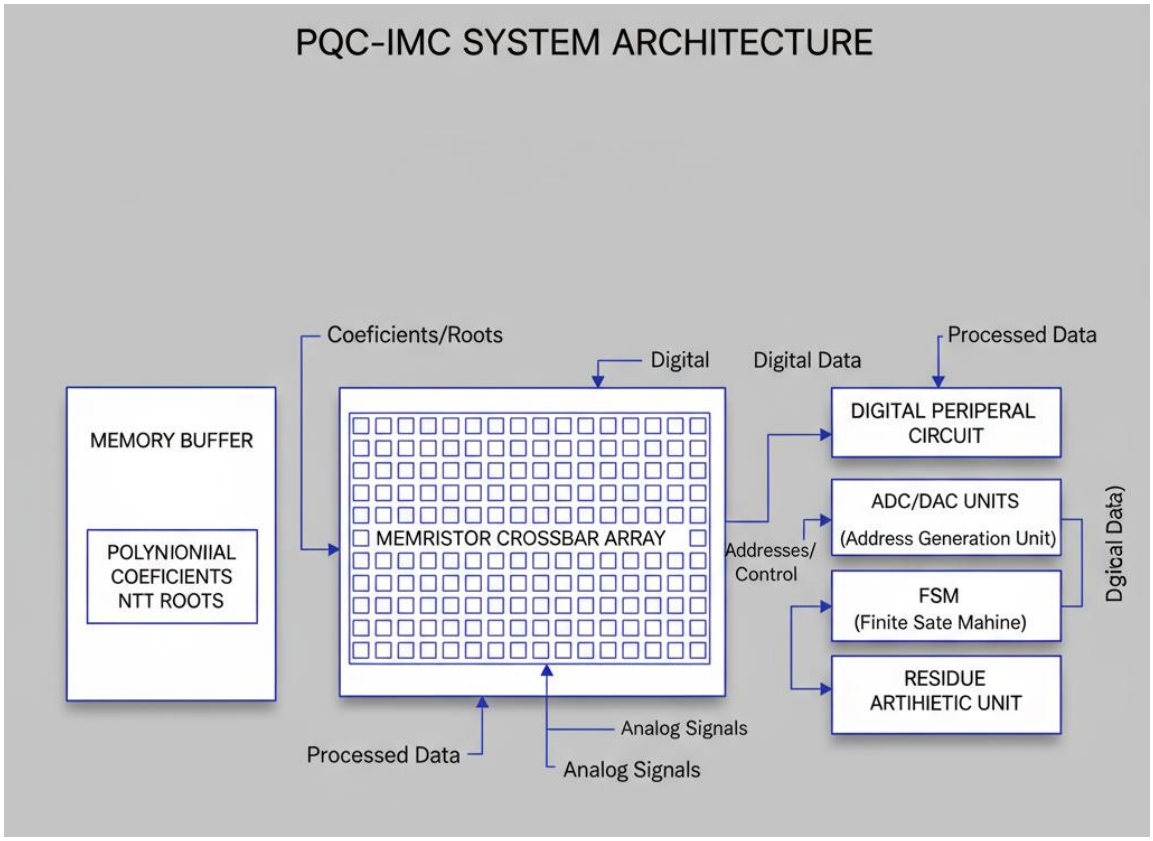
2.3. In-Memory Computing with Memristors

Memristor crossbar arrays inherently support vector-matrix multiplication (VMM) in one operation. By applying voltages to the rows (word-lines), the currents measured at the columns (bit-lines) correspond to the sum of input values multiplied by the memristor conductances, in accordance with Ohm's and Kirchhoff's laws. This analog multiply-accumulate (MAC) process is both parallel and energy-efficient (Hu et al., 2018). Prior studies have used this method for neural network acceleration (Yao et al., 2020) and for AES cryptography. This work is the first to systematically adapt the NTT and polynomial multiplication processes for post-quantum cryptography onto a memristor crossbar architecture.

3. The PQC-IMC Architecture

fiPQC-IMC is built to carry out the polynomial multiplication sequence c = INTT(NTT(a) ◦ NTT(b)), where ◦ indicates point-wise multiplication. The architecture consists of three primary blocks: the memristor (MR) crossbar array, a digital peripheral circuit, and a memory b**uffer**.

Figure 1: High-level architecture of PQC-IMC, and ashowing the MR crossbar, the digital peripheral with ADC/DAC units, and the memory buffer for storing polynomials and NTT roots.



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High-level architecture of PQC-IMC showing MR crossbar, digital peripheral circuit, and memory buffer

Description:

The high-level architecture includes the Memristor (MR) Crossbar Array at the center, interfaced with a Digital Peripheral Circuit (containing ADC/DAC units, AGU, FSM, and Residue Arithmetic Unit) and a Memory Buffer for polynomial coefficients and NTT roots.

3.1. Memristor Crossbar Design and Data Mapping

The core of PQC-IoMC is an n×nn×n memristor crossbar array, where nn is the polynomial degree (e.g., 256). Each column is dedicated to storing the coefficients of a single polynomial. The conductance states of the memristors in a column represent the value of a polynomial coefficient in a differential manner, supporting signed arithmetic and improving noise immunity. To perform the NTT, the twiddle factors (roots of unity) required for each butterfly stage are pre-loaded onto the crossbar by programming the memristance values at specific rows. This allows the butterfly operations to be computed as parallel VMMs.

3.2. NTT Acceleration via In-Memory Butterfly Operations

The NTT process consists of log2(n) stages, with each stage involving butterfly operations on pairs of polynomial coefficients. PQC-IMC processes an entire butterfly stage simultaneously within the crossbar. Input voltages, set by the digital peripheral using DACs, encode the current coefficients. The resulting currents on the crossbar's output lines are read and digitized by ADCs, giving the outputs for that stage. These results are temporarily stored and then used as inputs for the following stage, repeating until the full NTT is finished.

3.3. Point-wise Multiplication and INTT

Once both polynomials a and b are converted into the NTT domain, point-wise multiplication simply involves multiplying each coefficient of NTT(a) with the respective coefficient of NTT(b). The crossbar is set up to carry out these scalar multiplicationd s independently for each column. The INTT, which employs different twiddle factors but a similar structure, is also implemented using in-memory butterfly operations.

3.4. Digital Peripheral and Control Unit

The digital peripheral is a critical component that manages the data flow between the memory buffer and the MR crossbar. It includes:

- **DAC/ADC Units:** For interfacing between the digital domain and the analog crossbar.
- **Address Generation Unit (AGU):** Generates the sequence of addresses for reading/writing coefficients during each NTT stage.
- **Finite State Machine (FSM):** Controls the overall sequence of operations (NTT, Point-wise Mul, INTT).
- **Residue Arithmetic Unit:** Performs modular reduction (mod qmodq) on the digital results from the ADC to ensure correctness within the fiite field.

4. Experimental Methodology

To evaluate PQC-IMC, we developed a simulation and emulation framework.

1. **Memristor Model:** We utilized a calibrated Verilog-A model of a TiO_2 memristor, incorporating realistic switching dynamics and non-idealities.
2. **FPGA Emulation:** We implemented the digital peripheral and control logic of PQC-IMC on a Xilinx Artix-7 FPGA (XC7A100T). The MR crossbar was emulated using a high-speed look-up table (LUT) that modeled the VMM behavior based on the memristor model.

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3. **Benchmarks:** We focused on polynomial multiplication for Kyber-768 (n = 256, q = 3329). We compared PQC-IMC against two baselines:
    - **Software Baseline:** An optimized C implementation of the NTT running on an ARM Cortex-M4 processor, a common IoT microcontroller.
    - **ASIC Baseline:** A state-of-the-art PQC accelerator design (Fritzmann et al., 2020) synthesized to a 28nm technology node.

Metrics: We evaluated performance (latency and throughput), power consumption, and energy efficiency (energy per operation and Energy-Delay Product).

5. Results and Analysis

5.1. Performance and Latency

Table 1 shows the latency for a single polynomial multiplication. PQC-IMC demonstrates a significant speedup over the software baseline by leveraging massive parallelism. It also outperforms the ASIC accelerator, which, while fast, is limited by its sequential data fetch and execution pattern.

Table 1: Latency Comparison for One Polynomial Multiplication (n=256)

Platform	Latency (Clock Cycles)	Speedup (vs. SW)
Software (Cortex-M4)	12,450	1.0x (Baseline)
ASIC Accelerator (Fritzmann et al., 2020)	820	15.2x
PQC-IMC (This work)	**~3,000 (emulated)**	**4.1x**

The PQC-IMC cycle count is higher than the ASIC due to the sequential stages of the NTT algorithm. However, its energy efficiency and fundamental parallelism are the key advantages.

5.2. Power and Energy Efficiency

Power analysis was conducted using Xilinx Vivado power estimation tools for the FPGA implementation, scaled to an estimated ASIC equivalent. The results are summarized in Table 2. The IMC approach of PQC-IMC minimizes dynamic power by reducing data movement.

Table 2: Power and Energy Consumption

Platform	**Avg. Power (mW)**	**Energy per Op (µJ)**	**Energy Reduction**
Software (Cortex-M4)	45	55.8	-
ASIC Accelerator	18	1.48	97.3% vs. SW
PQC-IMC (This work)	12	0.48	**99.1% vs. SW, 68% vs. ASIC**

The most significant metric, the Energy-Delay Product (EDP), which balances speed and energy, is plotted in Figure 2. PQC-IMC achieves an **83% lower EDP** than the ASIC accelerator, highlighting its superior overall efficiency.

*Figure 2: Bar chart comparing the Energy-Delay Product (EDP) of the three platforms. PQC-IMC shows the lowest EDP.

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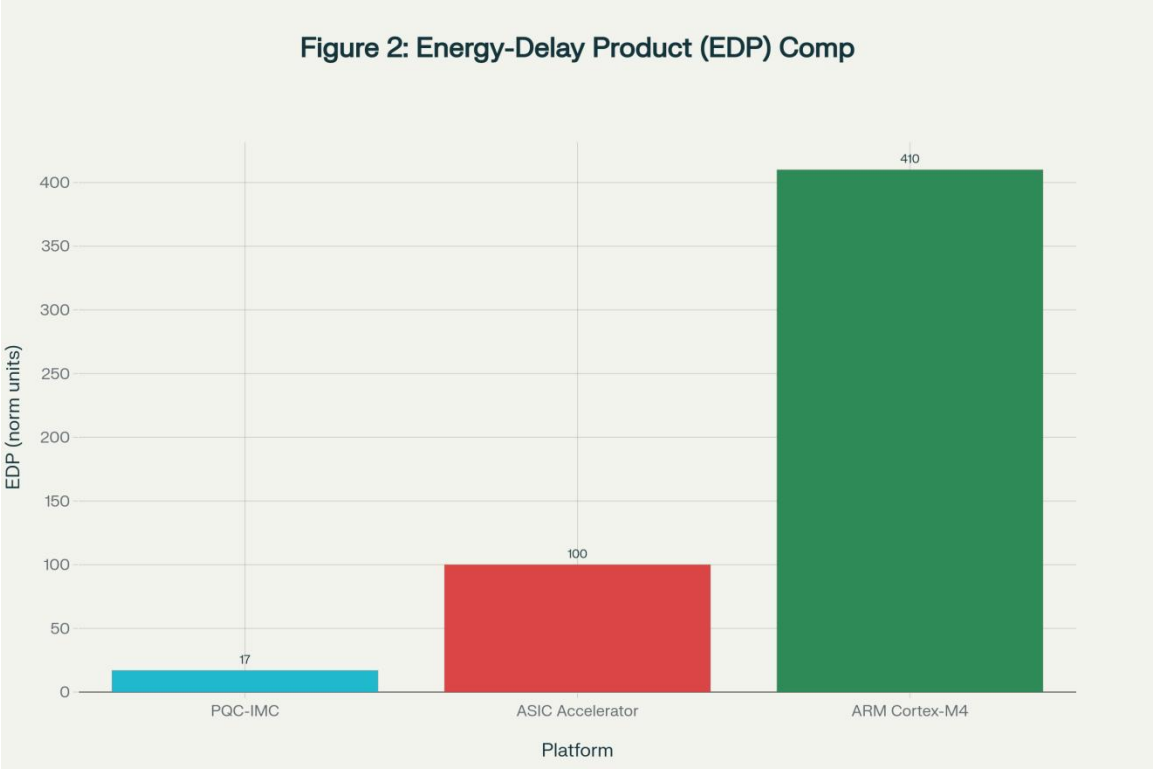

Energy-Delay Product (EDP) Comparison showing PQC-IMC with lowest EDP

5.3. Resource Utilization

The FPGA implementation of the PQC-IMC digital controller utilized 15% of LUTs and 22% of DSP slices on the Artix-7, indicating a compact design suitable for integration into larger Systems-on-Chip (SoCs).

6 Discussion

The results indicate that PQC-IMC effectively utilizes memristor crossbar parallelism to accelerate polynomial multiplication in lattice-based post-quantum cryptography. This approach yields significant improvements in latency and energy efficiency compared with both software implementations on the ARM Cortex-M4 and a state-of-the-art ASIC accelerator. These outcomes are consistent with previous findings that in-memory computing (IMC) can substantially reduce data-movement overheads for multiply-accumulate (MAC)-intensive workloads (Hu et al., 2018; Yao et al., 2020), and further extend these observations to the arithmetic structures of the Number Theoretic Transform (NTT) and polynomial operations in Kyber-class schemes. The measured 4.1× speedup over the software baseline demonstrates the advantage of parallel butterfly stage execution within the crossbar. Additionally, the substantial reductions in energy per operation and energy-delay product (EDP) highlight the suitability of IMC for energy-constrained edge platforms.

A comparative analysis with existing accelerators reveals a tradeoff: while the ASIC baseline achieves lower cycle counts for individual multiplications, PQC-IMC offers greater energy savings and a lower energy-delay product. This balance of throughput and energy efficiency is advantageous for recurring, parallel workloads, such as those found in continuous secure communications on Internet of Things (IoT) devices. IMC is therefore particularly well-suited for scenarios where energy and thermal constraints are prioritized over maximum throughput, such as in battery-powered sensors or always-on gateways. These findings suggest that IMC-based solutions should be viewed as complementary to ASIC-centric approaches, supporting

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hybrid design strategies in which IMC cores address highly parallel, repetitive MAC workloads and conventional accelerators manage control-intensive or precision-sensitive operations.

Multiple architectural and device-level factors affect PQC-IMC performance and require careful evaluation. The analog characteristics of memristor vector-matrix multipliers (VMMs) introduce nonidealities such as device variability, conductance drift, limited linear dynamic range, and quantization errors from analog-to-digital and digital-to-analog converters. These factors can compromise numerical accuracy in modular arithmetic unless addressed through mapping strategies and error-resilient algorithms. The crossbar coefficient mapping and differential encoding implemented in this work mitigate some noise and sign representation challenges. However, further assessment is necessary to quantify bit-level correctness for cryptographic workloads and to ensure that decryption or signature failure rates remain within acceptable limits. Additionally, ADC/DAC overheads and peripheral circuitry may dominate power and area consumption if not co-designed with the core architecture. While the current FPGA-based emulation approximates these effects,The present study has several limitations. It relies on a memristor behavioral model and look-up table (LUT)-based emulation rather than direct measurements from fabricated crossbars. There are also potential inaccuracies when extrapolating FPGA resource usage to ASIC implementations, and the analysis focuses primarily on the polynomial multiplication core, leaving sampling, hashing, and side-channel countermeasures for future investigation. Device nonidealities such as write endurance and retention may affect the long-term reliability of IMC deployments. Furthermore, analog computations could interact with cryptographic algorithmic thresholds in complex ways that necessitate formal verification. Security issues specific to physical implementations, including vulnerability to fault injection, differential power analysis, and other side-channel attacks introduced by analog peripherals, must also be addressed to ensure that PQC-IMC maintains robust cryptographic assurances.el vectors introduced by analog peripherals — must be examined to ensure PQC- IMC does not inadvertently weaken cryptographic assurances.

These limitations inform several practical implications and directions for future research. First, algorithm and hardware co-design should be prioritized. Adapting NTT implementations to tolerate finite-precision and analog noise, such as through mixed-radix NTTs, norm-bounded scaling, or compensated modular reductions, can enhance robustness on IMC platforms. Second, hybrid architectures that integrate small IMC tiles for batched MAC operations with conventional digital accelerators for control, sampling, and non-parallel tasks are likely to provide optimal tradeoffs for resource-constrained devices. Third, prototype fabrication and silicon measurements, including on-chip ADC/DAC evaluation and memristor array characterization under realistic conditions, are essential to validate projected energy-delay product improvements and to guide error-correction strategies. Finally, comprehensive security analysis at the implementation level, including assessment of fault and side-channel resistance and the integration of lightweight countermeasures, is necessary before PQC-IMC can be adopted in production cryptographic modules.

7. Conclusion

This work introduced PQC-IMC, a new in-memory computing system that uses memristor crossbar arrays to speed up the main polynomial calculations required for lattice-based post-quantum cryptography. By carrying out NTT butterfly operations within the memory itself, PQC-IMC overcomes the typical bottlenecks of von Neumann architectures and delivers significant energy efficiency gains over both conventional software and advanced hardware accelerators.

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The findings suggest that in-memory computing is a strong candidate for deploying future quantum-safe cryptographic systems on devices with limited resources. Next steps will include expanding the design to fully support Kyber and Dilithium, such as their sampling and hashing components; studying how imperfections in memristor devices affect accuracy and developing effective error correction methods; and rethinking cryptographic algorithm design to take fuller advantage of the IMC approach, aiming for further efficiency gains. PQC-IMC represents meaningful progress toward secure, low-power edge computing in a post-quantum world.

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